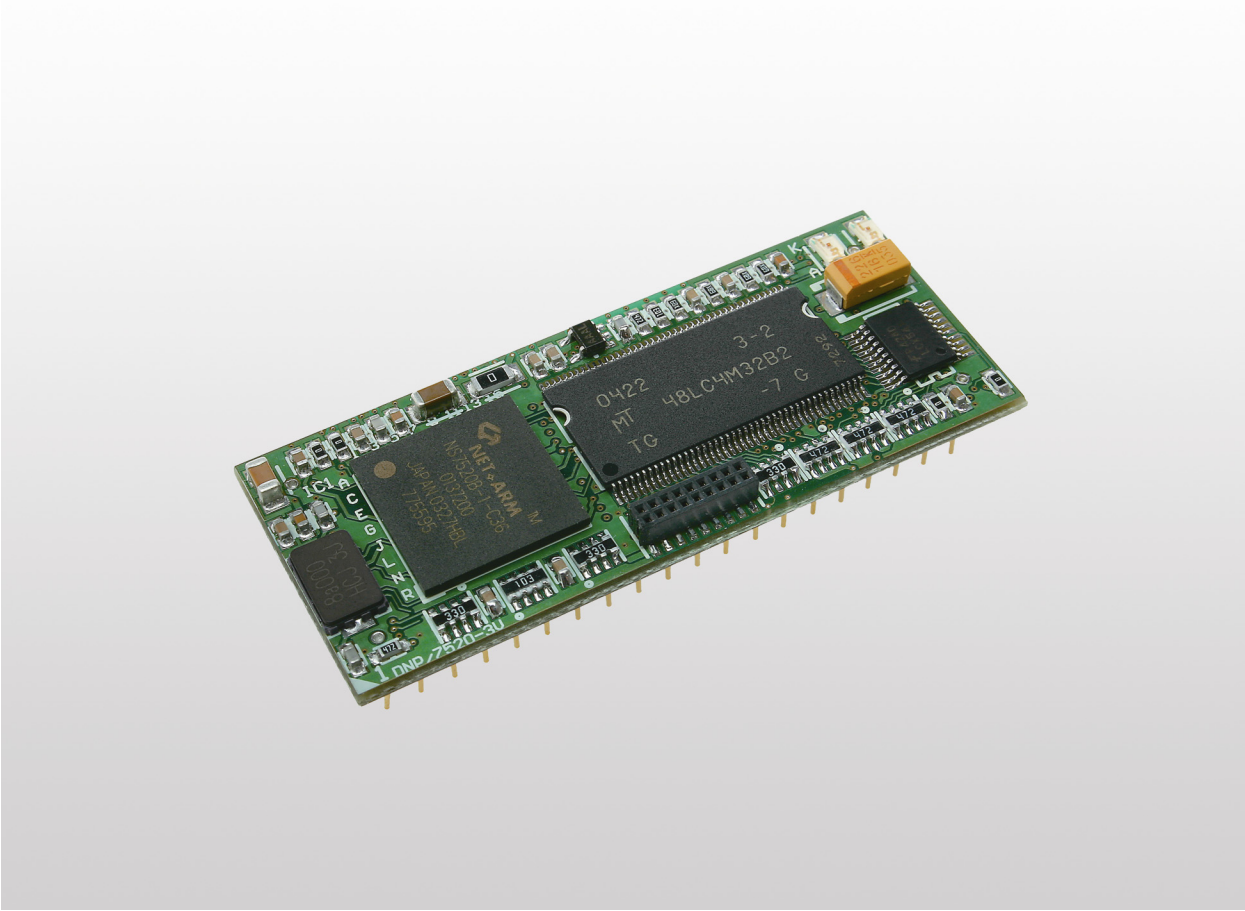
DIL/NetPC DNP/7520
Board Revision 1.1

Hardware Reference



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For further information regarding our products please visit us at www.dilnetpc.com

CONTENT

1 INTRODUCTION

This document describes the hardware components of the DNP/7520. For further information about the individual components of this product you may follow the links from our website at http://www.dilnetpc.com. Our website contains a lot of technical information, which will be updated in regular periods.

Figure 1 shows the block diagram of this small 32-bit embedded Linux computer.

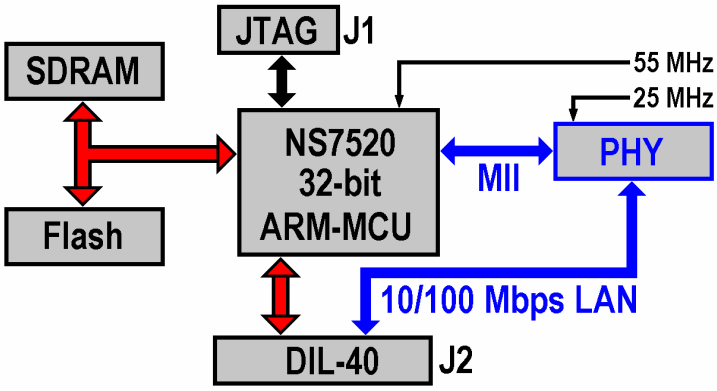


Figure 1: Block diagram of DNP/7520

The micro controller of the DIL/NetPC DNP/7520 is a NS7520 32-bit ARM MCU (Micro Controller Unit). This chip operates with a clock speed of 55 MHz. The NS7520 is a very complex ARM SoC chip (SoC = System-on-Chip, a special ASIC with ARM CPU). It consists – besides the ARM7TDMI processor core – of a diverse appropriable bus interface, a DMA controller, two universal UART/HDLC and SPI units, a 10/100 Mbps Ethernet MAC controller, GPIO and timer functions as well as an interrupt controller. The NS7520 is built in a small BGA case with an edge length of 13 x 13 mm and 177 pins.

The memory equipment of the DIL/NetPC DNP/7520 consists of a 16 MByte SDRAM and an 8 MByte Flash memory chip. The SDRAM serves for the embedded Linux operating system as working memory and RAM disk. The permanent Flash memory area hosts the boot loader (U-Boot) and the Linux root file system on the basis of a JFFS2 (Journaling Flash File System, Version 2).

The internal 10/100 Mbps Ethernet MAC controller of the 32-bit ARM MCU is connected with an external PHY chip. MAC and PHY together form the Ethernet LAN interface of the DIL/NetPC DNP/7520.

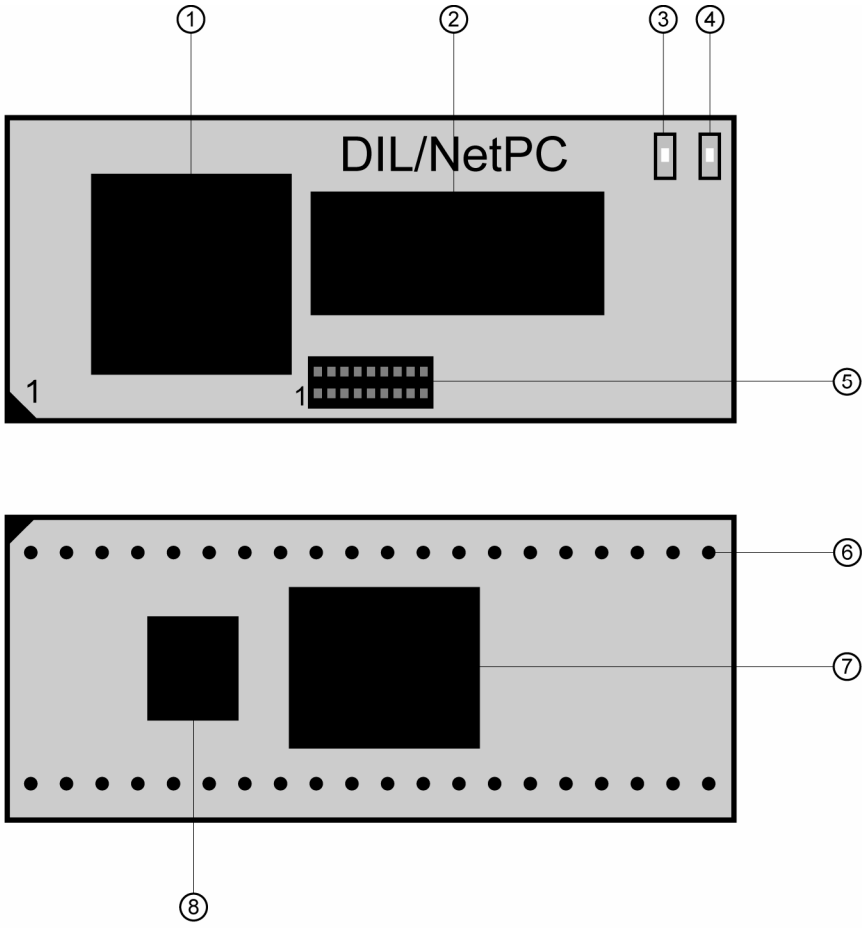
For hardware test and software debugging tasks the NS7520 disposes the ARM-typical embeddedICE interface. This JTAG-compliant interface is accessible via a small special connector on the printed circuit board of the DIL/NetPC DNP/7520 (J1 in the block diagram).

The 40-pin DIL connector J2 serves as a circuit expansion and supplies a 3.3 VDC supply voltage to the DIL/NetPC DNP/7520. The Ethernet signals of the DIL/NetPC DNP/7520 are also leaded to J2.

1.1 Features DNP/7520

- One 32-bit ARM-MCU with 55 MHz
- One 40-pin DIL connector
- One JTAG connector
- 16 Mbyte SDRAM memory
- 8 Mbyte Flash memory
- Two Ethernet activity LEDs (one for 10 Mbps and one for 100 Mbps)
- One 10/100 Mbps Ethernet MAC controller
- One Ethernet PHY chip
- Size 55 x 23 mm

2 BOARD LAYOUT



① 32-bit ARM-MCU
② 16 MByte SDRAM memory
③ 100 Mbps Ethernet activity LED
④ 10 Mbps Ethernet activity LED
⑤ J1 - JTAG connector
⑥ J2 - DIL-40 connector
⑦ 8 MByte Flash memory
⑧ Ethernet PHY chip

Figure 2: Board layout DNP/7520

3 PINOUTS

3.1 DIL-40 Connector – J2

Pin	Name	Function	Group
1	PA0	Parallel I/O, Port A, Bit 0	GPIO
2	PA1	Parallel I/O, Port A, Bit 1	GPIO
3	PA2	Parallel I/O, Port A, Bit 2	GPIO
4	PA3	Parallel I/O, Port A, Bit 3	GPIO
5	PA4	Parallel I/O, Port A, Bit 4	GPIO
6	PA5	Parallel I/O, Port A, Bit 5	GPIO
7	PA6	Parallel I/O, Port A, Bit 6	GPIO
8	PA7	Parallel I/O, Port A, Bit 7	GPIO
9	SD0	Expansion Bus, Data Bit 0	GPE
10	SD1	Expansion Bus, Data Bit 1	GPE
11	SD2	Expansion Bus, Data Bit 2	GPE
12	SD3	Expansion Bus, Data Bit 3	GPE
13	SD4	Expansion Bus, Data Bit 4	GPE
14	SD5	Expansion Bus, Data Bit 5	GPE
15	SD6	Expansion Bus, Data Bit 6	GPE
16	SD7	Expansion Bus, Data Bit 7	GPE
17	RESIN#	Reset Input (Low Active)	---
18	CS1#	Expansion Bus, Chip Select Output 1 (Low Active)	GPE
19	CS2#	Expansion Bus, Chip Select Output 2 (Low Active)	GPE
20	GND	Ground	---
21	RCM	RCM (Remote Console Mode) Input	GPIO
22	TX+	10/100 Mbps Ethernet LAN Interface, TX+ Pin	LAN
23	TX-	10/100 Mbps Ethernet LAN Interface, TX- Pin	LAN
24	RX+	10/100 Mbps Ethernet LAN Interface, RX+ Pin	LAN
25	RX-	10/100 Mbps Ethernet LAN Interface, RX- Pin	LAN
26	TXD2	COM2 Serial Port, TXD Output Pin	SIO
27	RXD2	COM2 Serial Port, RXD Input Pin	SIO
28	NC	Not Connected	SIO
29	VCCOUT	3.3 VDC Output	SIO
30	DSR1	COM1 Serial Port, DSR Input Pin	SIO
31	DCD1	COM1 Serial Port, DCD Input Pin	SIO
32	RTS1	COM1 Serial Port, RTS Output Pin	SIO
33	CTS1	COM1 Serial Port, CTS Input Pin	SIO
34	TXD1	COM1 Serial Port, TXD Output Pin	SIO
35	RXD1	COM1 Serial Port, RXD Input Pin	SIO
36	SA0	Expansion Bus, Address Bit 0	GPE
37	SA1	Expansion Bus, Address Bit 1	GPE
38	WR#	Expansion Bus, Write Signal (Low Active)	GPE
39	RD#	Expansion Bus, Read Signal (Low Active)	GPE
40	VCC	3.3 VDC Power Input	---

Table 1: Pinout DIL-40 connector

Note: The arrangement of the signals in groups has compatibility reasons. Other products of SSV with DIL-40 pinout are fully or conditionally pin compatible to the DIL/NetPC DNP/7520 by observance of the corresponding application note.

3.2 JTAG Connector – J1

You can use an adapter to convert the miniature JTAG connector of the DNP/7520 to the common 2.54 mm raster. Then standard JTAG connector modules can be used.

Manufacturer of the JTAG connector (1 mm grid / 2 lines / 2 x 9 pins) is W+P Products (http://www.wppro.com), type 7091-18-10-ST.

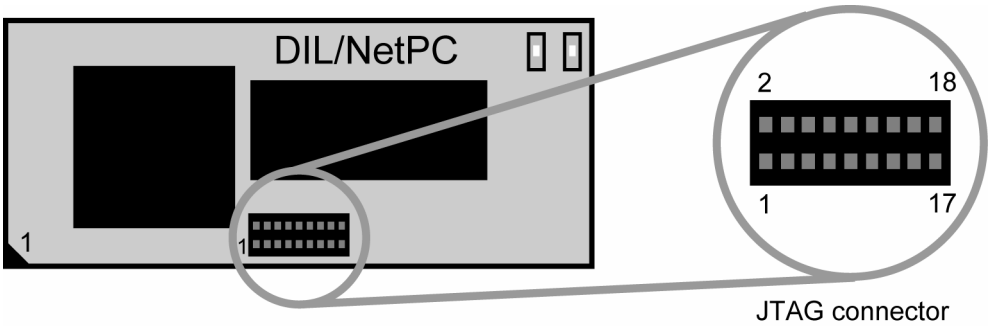


Figure 3: Position of JTAG connector on the DNP/7520

Pin	Name	Function
1	VCC	Power (3.3 VDC I/O Voltage)
2	GND	Ground
3	---	Not Connected
4	TMS#	Test Mode Select
5	PWRGD#	Power Good (internal CPU Reset)
6	TRST#	Test Reset
7	TDI	Test Data In
8	TCK	Test Clock
9	---	Not Connected
10	TDO	Test Data Out
11	---	Not Connected
12	---	Not Connected
13	---	Not Connected
14	---	Not Connected
15	---	Not Connected
16	---	Not Connected
17	---	Not Connected
18	---	Not Connected

Table 2: Pinout JTAG connector

3.3 JTAG Interface

The JTAG signals of the DNP/7520 connector J1 are directly connected to the JTAG TAP controller of the NS7520 32-bit ARM-MCU.

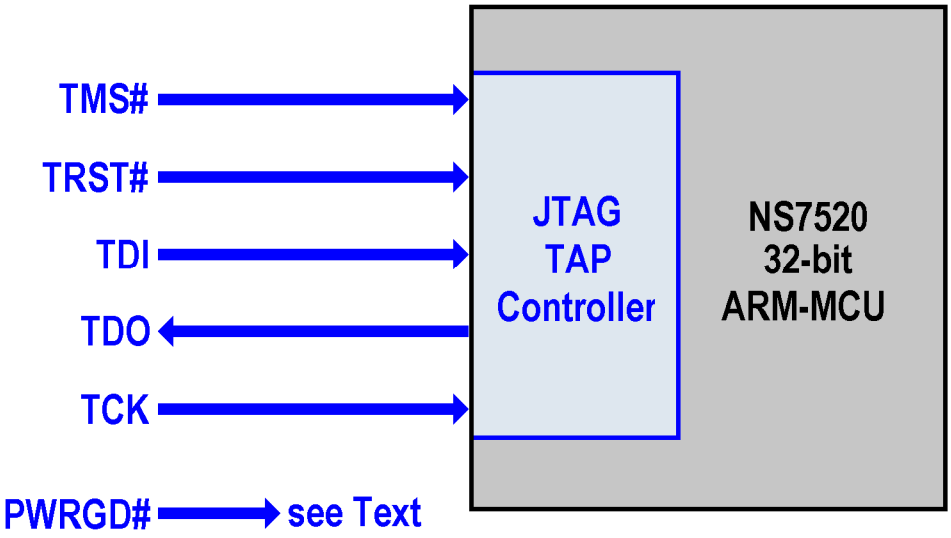


Figure 4: DNP/7520 JTAG interface

The signal PWRGD# generates a CPU reset. Some JTAG debuggers are using this signal for CPU/core reset operations.

4 MECHANICAL DIMENSIONS

All length dimensions have a tolerance of 0.5 mm.

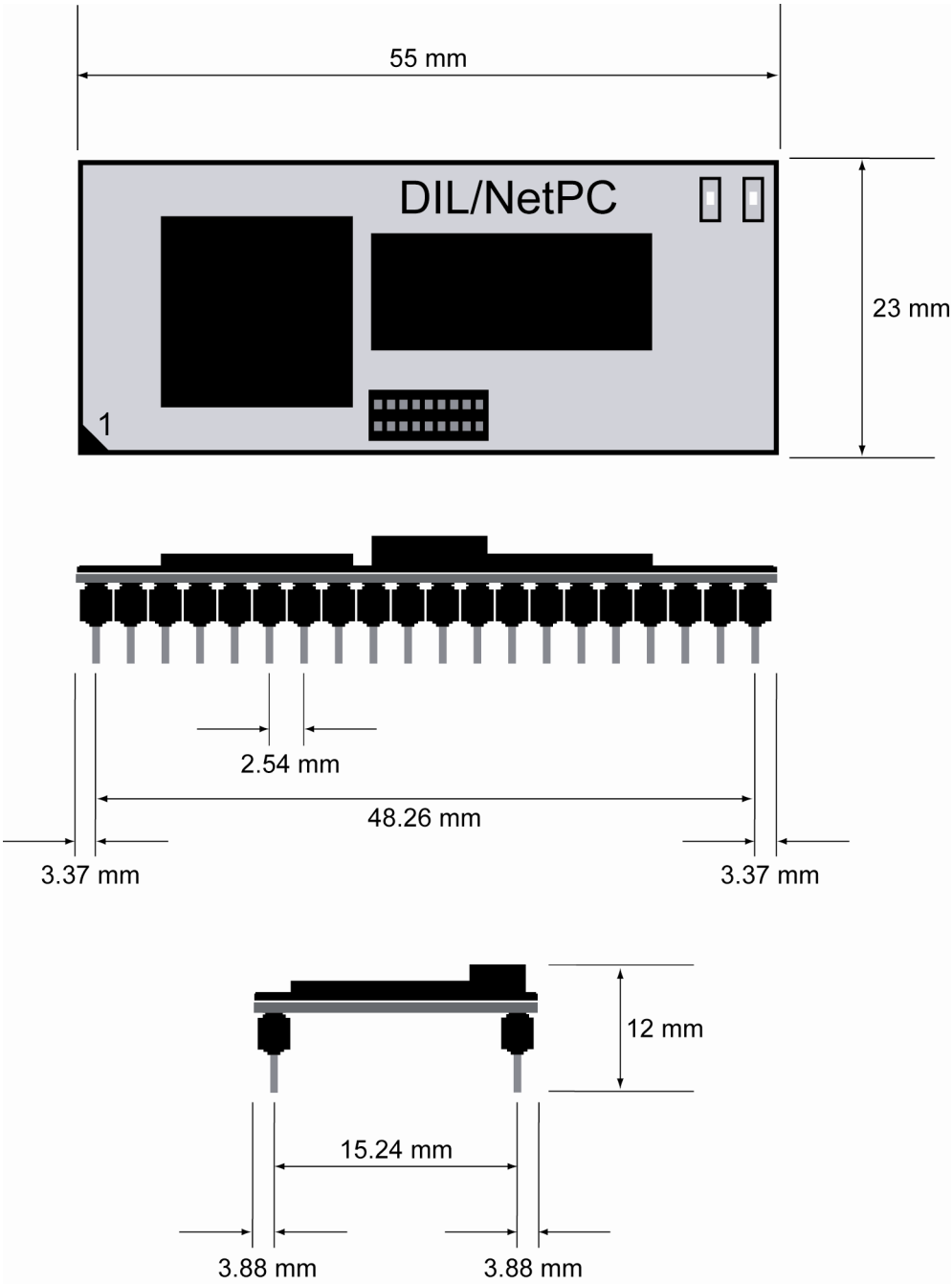


Figure 5: Mechanical dimensions of DNP/7520

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DOCUMENT HISTORY

Revision	Date	Remarks	Name
1.0	2005-05-04	first version	WBU