

DIL/NetPC DNP/5282 ***Board Revision 1.1***

Hardware Reference



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1 INTRODUCTION

This document describes the hardware components of the DNP/5282. For further information about the individual components of this product you may follow the links from our website at <http://www.dilnetpc.com>. This website contains a lot of technical information, which will be updated in regular periods.

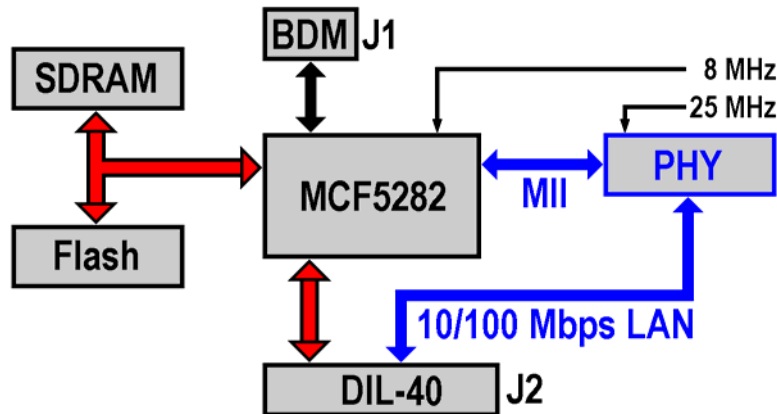


Figure 1: Block diagram of DNP/5282

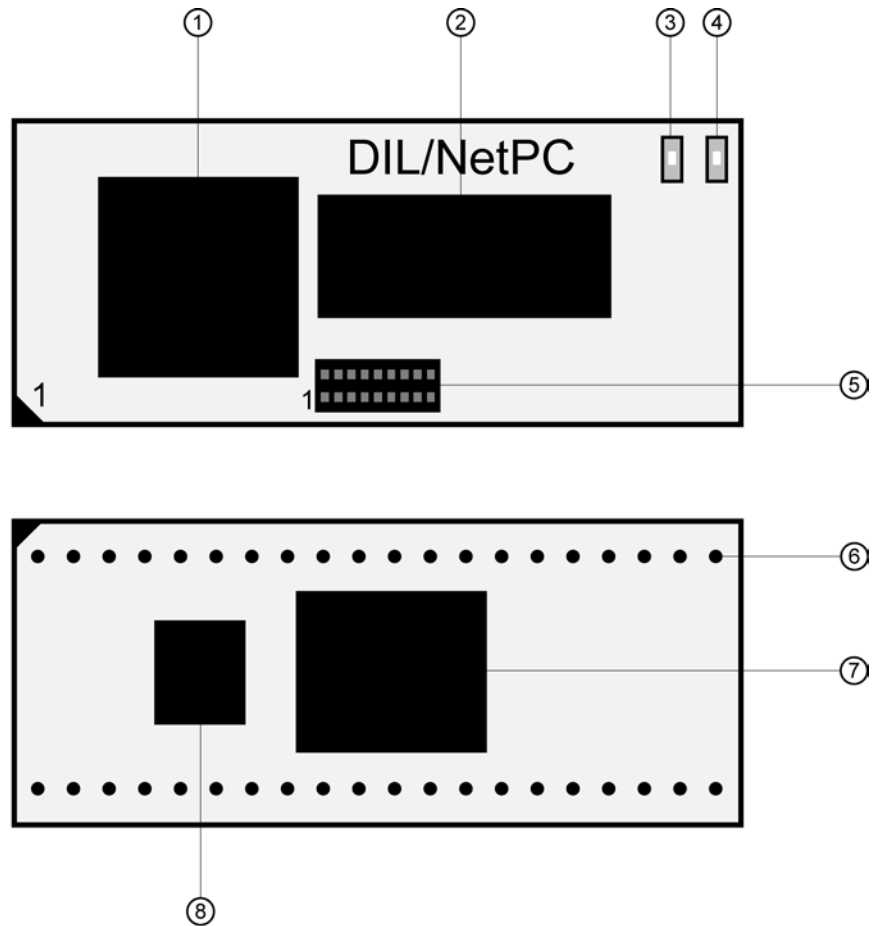
Figure 1 shows the block diagram of the DIL/NetPC DNP/5282. The DNP/5282 is built around Motorola's 32-bit ColdFire MCF5280/MCF5282 microcontroller unit (MCU) running with 66 MHz. The external main components around the ColdFire are one Flash memory chip with 8 Mbytes, one 16-MByte SDRAM memory chip, and one 10/100 Mbps Ethernet PHY (the Ethernet MAC is a part of the ColdFire MCU).

The 66 MHz clock speed of the DIL/NetPC DNP/5282 comes from a 8 MHz clock source. The DNP/5282 offers only two connectors: J1 (BDM Interface) and J2 (40-pin DIL Connector).

1.1 Features DNP/5282

- Motorola 32-bit MCF528x ColdFire with 66 MHz Clock Speed
- 63 MIPS (Dhrystone 2.1)
- 16 MByte SDRAM Memory, 8 MByte FLASH Memory
- 10/100 Mbps Ethernet LAN Interface
- Two Ethernet LAN Status LEDs
- Two asynchronous Serial Ports (one with all Handshakes)
- One I2C Interchip Bus Interface
- One Queued Serial Peripheral Interface (SPI) with two Chip Select Outputs
- One CAN Interface (Supports CAN Protocol Specification 2.0B)
- 20-bit General Purpose high-speed Parallel I/O
- Programmable General Purpose Timers and Watchdog Timer
- Motorola BDM (Background Debug Mode) Interface for In-Circuit Debugging
- In-System Programming Features
- Software compatible with DNP/5280 and PNP/5280
- 40-pin JEDEC DIL Connector, 2.54mm Centers
- 3.3 Volt Low Power Design, Supply Voltage 3.3 VDC (+- 5%)
- Supply Current 300 mA typ. at 66 MHz
- Size 55mm * 23mm

2 BOARD LAYOUT



- | | |
|----------------------------------|-------------------------|
| ① 32-bit Coldfire MCU | ⑤ J1 - BDM connector |
| ② 16 MByte SDRAM memory | ⑥ J2 - DIL-40 connector |
| ③ 10 Mbps Ethernet activity LED | ⑦ 8 MByte Flash memory |
| ④ 100 Mbps Ethernet activity LED | ⑧ Ethernet PHY chip |

Figure 2: Board layout DNP/5282

3 PINOUTS

3.1 DIL-40 Connector – J2

Pin	Name	Group	Function
1	PA0	PIO	Parallel I/O, Port A, Bit 0
2	PA1	PIO	Parallel I/O, Port A, Bit 1
3	PA2	PIO	Parallel I/O, Port A, Bit 2
4	PA3	PIO	Parallel I/O, Port A, Bit 3
5	PA4	PIO	Parallel I/O, Port A, Bit 4
6	PA5	PIO	Parallel I/O, Port A, Bit 5
7	PA6	PIO	Parallel I/O, Port A, Bit 6
8	PA7	PIO	Parallel I/O, Port A, Bit 7
9	PB0	PIO	Parallel I/O, Port B, Bit 0
10	PB1	PIO	Parallel I/O, Port B, Bit 1
11	PB2	PIO	Parallel I/O, Port B, Bit 2
12	PB3	PIO	Parallel I/O, Port B, Bit 3
13	PB4	PIO	Parallel I/O, Port B, Bit 4
14	PB5	PIO	Parallel I/O, Port B, Bit 5
15	PB6	PIO	Parallel I/O, Port B, Bit 6
16	PB7	PIO	Parallel I/O, Port B, Bit 7
17	RESIN	RESET	Reset Input (Low Active)
18	SPI.CS1	SPI	QSPI Chip Select Output 1
19	SPI.CS2	SPI	QSPI Chip Select Output 2
20	GND	---	Ground
21	RCM	---	RCM (Remote Console Mode) Input
22	TX+	LAN	10/100 Mbps LAN, TX+ Pin
23	TX-	LAN	10/100 Mbps LAN, TX- Pin
24	RX+	LAN	10/100 Mbps LAN, RX+ Pin
25	RX-	LAN	10/100 Mbps LAN, RX- Pin
26	TXD2	SIO	COM2 Serial Port, TXD Pin
27	RXD2	SIO	COM2 Serial Port, RXD Pin
28	RI1	SIO	COM1 Serial Port, RI Pin
29	DTR1	SIO	COM1 Serial Port, DTR Pin
30	DSR1	SIO	COM1 Serial Port, DSR Pin
31	DCD1	SIO	COM1 Serial Port, DCD Pin
32	RTS1	SIO	COM1 Serial Port, RTS Pin
33	CTS1	SIO	COM1 Serial Port, CTS Pin
34	TXD1	SIO	COM1 Serial Port, TXD Pin
35	RXD1	SIO	COM1 Serial Port, RXD Pin
36	PC0	PIO	Parallel I/O, Port C, Bit 0
37	PC1	PIO	Parallel I/O, Port C, Bit 1
38	PC2	PIO	Parallel I/O, Port C, Bit 2
39	PC3	PIO	Parallel I/O, Port C, Bit 3
40	Vcc	---	3.3 Volt Power Input

Table 1: Pinout DIL-40 connector

Note: The arrangement of the signals in groups has compatibility reasons. Other products of SSV with DIL-40 pinout are fully or conditionally pin compatible to the DIL/NetPC DNP/5282 by observance of the corresponding application note.

3.2 Function Multiplexing with DIL-40 Connector

Some pins of the 40-pin DIL connector of the DNP/5282 have multiple meanings. The pins have a primary and a secondary function (function multiplexing). The primary functions correspond with the standard pinout of the 40-pin DIL connector as shown in **table 1**. The secondary functions are shown in **table 2** below.

Pin	Name	Primary functions	Secondary functions
13	PB4	Parallel I/O, Port B, Bit 4	SCL (I2C)
14	PB5	Parallel I/O, Port B, Bit 5	SDA (I2C)
15	PB6	Parallel I/O, Port B, Bit 6	CANTX (CAN)
16	PB7	Parallel I/O, Port B, Bit 7	CANRX (CAN)
36	PC0	Parallel I/O, Port C, Bit 0	QSPIDO (SPI)
37	PC1	Parallel I/O, Port C, Bit 1	QSPIDI (SPI)
38	PC2	Parallel I/O, Port C, Bit 2	QSPICLK (SPI)
39	PC3	Parallel I/O, Port C, Bit 3	QSPICS0 (SPI)

Table 2: DNP/5282 function multiplexing

3.3 PIO-Mapping

The 20 Signals for the DNP/5282-Parallel-I/O (PIO) are realized through different function units of the MCF528x. The following table shows the assignment. Pin names for the MCF528x-case (256-pin MAPBGA) are listed in the third column. Please see the MCF528x ColdFire microcontroller user manual R.0.1 (MCF5282UM/D) for further details.

Pin	Name	MCF528x-Pinfunction	MCF528x-Pin
1	PA0	AN52	R4
2	PA1	AN53	T4
3	PA2	AN55	P3
4	PA3	AN56	R3
5	PA4	AN0	T3
6	PA5	AN1	R2
7	PA6	AN2	T2
8	PA7	AN3	R1
9	PB0	GPTA0	N13
10	PB1	GPTA1	P13
11	PB2	GPTA2	R13
12	PB3	GPTA3	T13
13	PB4	SCL	E15
14	PB5	SDA	E14
15	PB6	CANTX	E13
16	PB7	CANRX	D16
36	PC0	QSPIDO	F13
37	PC1	QSPIDI	E16
38	PC2	QSPICLK	F14
39	PC3	QSPICS0	F15

Table 3: DNP/5282 PIO-mapping

3.4 COM Port Mapping

The 10 signals for the two DNP/5282 COM ports are realized with different function units of the MCF528x ColdFire MCU. **Table 4** shows the assignment.

Pin	Name	MCF528x-pinfunction	MCF528x-pin	Source
26	TXD2	UTXD1	P7	UART
27	RXD2	URXD1	R7	UART
28	RI1	DTIN3	K16	GPIO
29	DTR1	DTOUT3	K15	GPIO
30	DSR1	DTIN2	K14	GPIO
31	DCD1	DTOUT2	K13	GPIO
32	RTS1	DTIN1	J15	UART
33	CTS1	DTOUT0	J13	UART
34	TXD1	UTXD0	T7	UART
35	RXD1	URXD0	N6	UART

Table 4: DNP/5282 COM port mapping

The third column lists the pin-names for the MCF528x case (256-pin MAPBGA).

The fourth column shows the source of each pin. The COM1 port is not entirely realized through the signals of the MCF528x UART0. The missing signals are implemented via GPIOs (general purpose I/O pins).

These MCF528x signals have to be configured as PIO (parallel I/O) for the COM1 usage.

3.5 Memory Mapping

Function Unit	Start Address	End Address	Access Format
SDRAM	0x0000.0000	0x00FF.FFFF	32 Bits
SRAM (intern)	0x2000.0000	0x2000.FFFF	32 Bits
IBSBAR	0x4000.0000	0x7FFF.FFFF	32 Bits
Flash (MCF528x intern)	0xF000.0000	0xF007.FFFF	32 Bits
Flash	0xFF80.0000	0xFFFF.FFFF	16 Bits

Table 5: DNP/5282 memory mapping

In memory area **IBSBAR** the SFRs (special function register) of the Motorola ColdFire MCF528x microcontroller are addressable.

User programs can only be loaded from 0x0001:0000 into the memory.

The DNP/5282 comes with a ROM monitor ex works. This ROM monitor needs a memory area in Flash and SDRAM each.

Function Unit	Startaddress	Endaddress
dBUG ROM Monitor Code-Area	0xFF80.0000	0xFF83.FFFF
dBUG ROM Monitor Data-Area	0x0000.0000	0x0000.FFFF

Table 6: DNP/5282 reserved areas for the ROM monitor

3.6 BDM Connector – J1

You can use an adapter to convert the miniature BDM connector of the DNP/5282 to the common 2.54 mm raster. Then standard BDM connector modules can be used.

Manufacturer of the BDM connector (1 mm grid / 2 lines / 2 x 9 pins) is W+P Products (<http://www.wpro.com>), type 7091-18-10-ST.

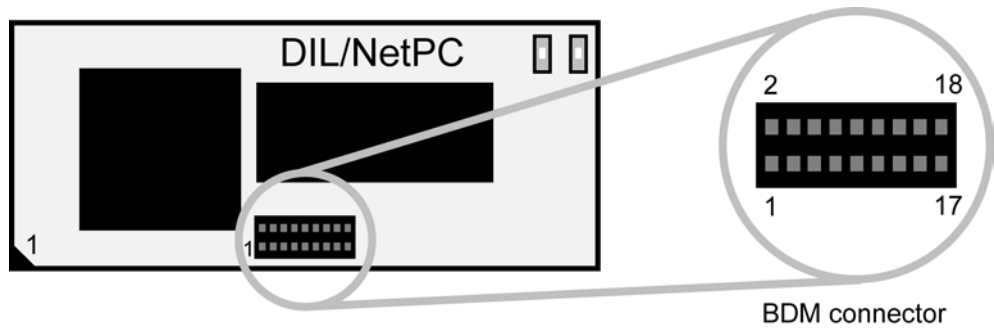


Figure 3: Position of BDM connector on the DNP/5282

Pin	Name	Function
1	VIO (3.3 VDC I/O Voltage)	Power
2	GND	Ground
3	TA#	Background Debug Mode
4	BKPT#	Background Debug Mode
5	Reset#	Background Debug Mode
6	DSCLK#	Background Debug Mode
7	DSI#	Background Debug Mode
8	TCLK	Background Debug Mode
9	PST3	Background Debug Mode
10	DS0	Background Debug Mode
11	PST2	Background Debug Mode
12	DDATA3	Background Debug Mode
13	PST1	Background Debug Mode
14	DDATA2	Background Debug Mode
15	PST0	Background Debug Mode
16	DDATA1	Background Debug Mode
17	PSTCLK	Background Debug Mode
18	DDATA0	Background Debug Mode

Table 7: Pinout BDM connector

4 MECHANICAL DIMENSIONS

All length dimensions have a tolerance of 0.5 mm.

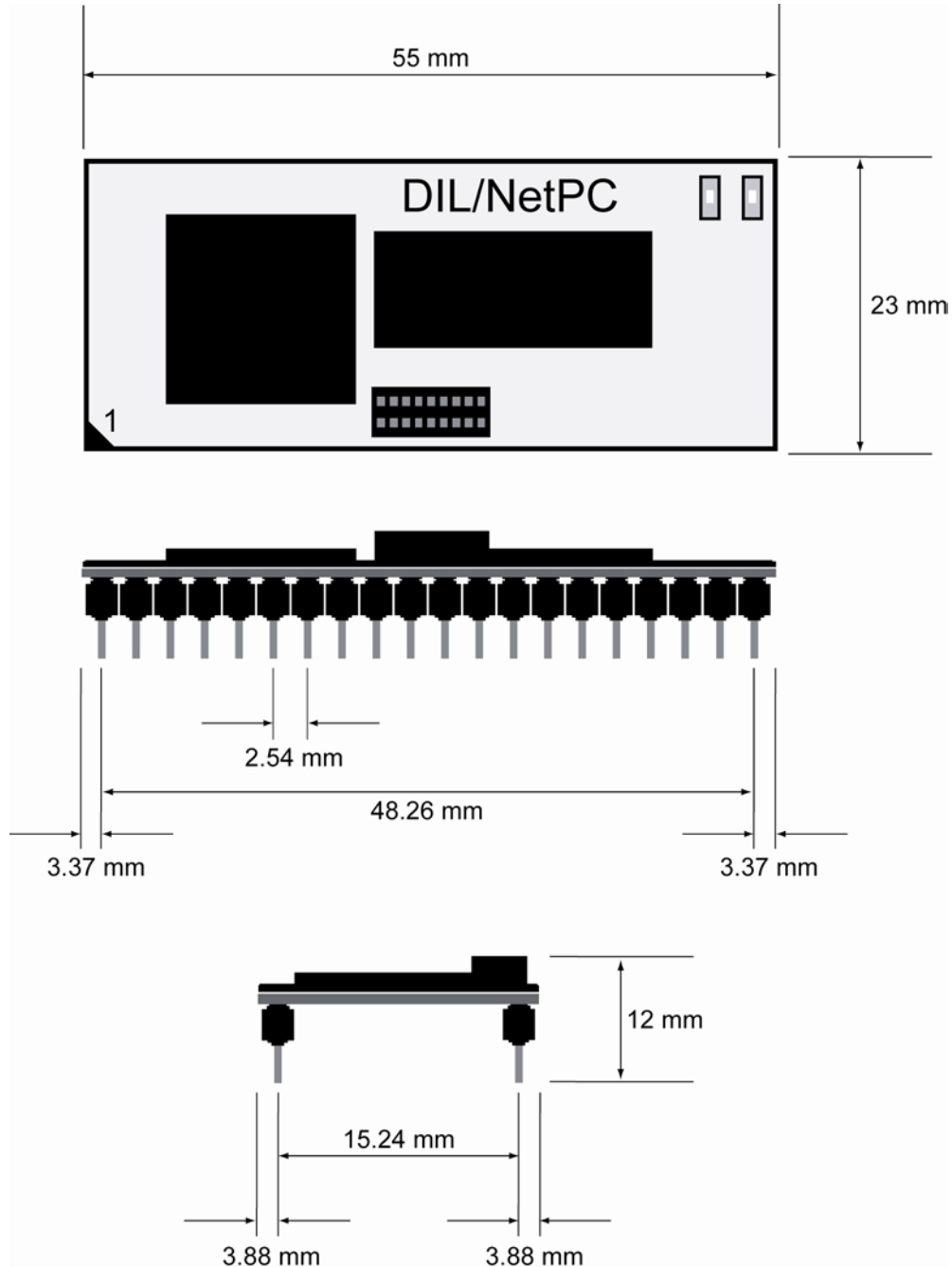


Figure 4: Mechanical dimensions of DNP/5282

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DOCUMENT HISTORY

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1.0	2005-06-29	First version	WBU
1.1	2005-07-05	Some Error corrections	KDW

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